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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/682,688	10/05/2001	Christos J. Georgiou	85773-259CIP	8979

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EXAMINER	
JOO, JOSHUA	

ART UNIT	PAPER NUMBER
2154	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/682,688	GEORGIOU ET AL.	
	Examiner	Art Unit	
	Joshua Joo	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-18 are presented for examination.

2. Claims 1-18 are rejected.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-12, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin, US Patent #6,393,026 and in view of Adiletta et al, US Patent #6,606,704 (Adiletta hereinafter).

5. As per claim 1, Irwin teaches of a multiprocessor system, where data packet processing is distributed to a plurality of processors, in which each processor has memory. Irwin's invention comprises of:

a) A plurality of programmable processors, each processor fully executing programs, thread units within a processor being assigned processing of various protocol functions in a parallel/pipelined fashion; and (Col 6, lines 17-26; Col 7, lines 15-20, 40-62. System comprises of programmable computing nodes for executing multiple threads in parallel processing. Individual computing nodes can execute any given procedure.);

b) A hardwired logic front end connected to a network interface for receiving and transmitting data, said hardwired logic performing time critical operations and communicating received data to and data to be transmitted from said plurality of programmable processors.

(Col 7, lines 56-61; Col 8, lines 8-11; Col 9, lines 33-46; Col 11, lines 9-13. I/O node of the Central Control Unit (CCU) receives and transmits data packets from networks. The I/O node also communicates received data to and data to be transmitted from the computing nodes. Program counter is initialized for the received data packet.).

6. Irwin does not specifically teach of each processor having multiple thread units, each thread unit capable of fully executing programs.

7. Adiletta teaches an invention for a parallel multithreaded processor, where the processor has a plurality of microengines. Each microengine has the capability of processing four hardware threads (Col 3, lines 20-30).

8. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Irwin and Adiletta because both inventions deal with multithreaded parallel processing. The teachings of Adiletta for each processing engine to possess hardware to process multiple threads improve the invention of Irwin by allowing Irwin's data processing system to process large amounts of data as taught by Adiletta.

9. As per claim 2, Irwin teaches the system recited in claim 1, wherein each of said programmable processors includes on-chip embedded memory for storing status and control information of current network traffic and for storing received data and data to be transmitted (Col 5, lines 50-67; Col 7, lines 56-63; Col 8, lines 14-17; Col 10, lines 1-19. Each computing node has memory and buffer to queue received information. The computing nodes store received data packets and transmits the data for processing. The computing nodes have packet forwarding programs loaded in the memory used for procedures such as congestion control and performance monitoring.).

10. As per claim 3, Irwin teaches the system recited in claim 2, said embedded memory contains an area dedicated for packet storage, an area where the payload and headers of frames are stored, an area for storing control and status blocks, an area where various protocol specific information and the current status of the network traffic is stored, and an area for working queues, as well as any other information required (Col 5, lines 50-67; Col 7, lines 56-63; Col 8, lines 1-17, 37-60; Col 10, lines 5-7. The computing nodes have memory, and FIFO buffer for queuing received information. The computing nodes have protocol specific information and procedures for translation, scheduling, and classification, which includes header parameters. The computing nodes store received data packets and have packet forwarding programs used for procedure such as congestion control and performance monitoring.).

11. As per claim 4, Irwin teaches the system recited in claim 3, wherein a beginning address of an inbound data block (IBDB) is added to the master input queue by an input processing unit which manages an IBDB memory area, a "master" thread stored in the master input queue assigning incoming frames to one of a fixed number of threads performing a network protocol, frame dispatching being performed by a workload allocation function which may include workload balancing functionality (Col 6, lines 56-61; Col 7, lines 56-67; Col 10, lines 5-16. As each packet arrives through the I/O node, the master node stores the packet in a buffer and assigns a counter to the program packet. The program packet defines a thread such that that a node executes a queue of procedural calls. The master node performs workload allocation, which includes workload balancing. The master node may limit the number of threads created in a system.).

12. As per claim 5, Irwin teaches the system recited in claim 2,wherein said programmable processors include an on-chip connecting the embedded memory and said multiple thread units (Fig. 7; Col 6, lines 5-16; Col 7, lines 56-61; Col 12, lines 26-27. Processor has multithread hardware connected to memory.).

13. Irwin does not specifically teach of each programmable processor having multiple thread units.

14. Adiletta teaches an invention for a parallel multithreaded processor, where the processor has a plurality of microengines. Each microengine has the capability of processing four hardware threads (Col 3, lines 20-30).

15. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Irwin and Adiletta because both inventions deal with multithreaded parallel processing. The teachings of Adiletta for each processing engine to possess hardware to process multiple threads improve the invention of Irwin by allowing Irwin's data processing system to process large amounts of data as taught by Adiletta.

16. As per claim 6, Irwin teaches the system recited in claim 5, wherein each of said multiple thread units comprises a register file, a program counter, an arithmetic logic unit, and logic for instruction fetching, decoding, and dispatching (Col 5, lines 50-55, 59-67; Col 6, lines 3-16; Col 11, lines 6-8, 49-64. Thread unit comprises of a register file, counter, and logic for fetching, decoding, and dispatching. An ALU is inherent since the processor executes algorithms.).

17. As per claim 7, Irwin teaches the system recited in claim 5, wherein on-chip high-speed interconnect is implemented as a ring (Col 7, line 45. Interconnect is implemented as a ring.).

18. As per claim 8, Irwin teaches the system recited in claim 5, wherein the on-chip high-speed interconnect is implemented as dual counter rotating rings (Col 7, lines 47-48; Col 9, lines 51-52. Interconnect is a dual ring to provide bidirectional communication to provide the shortest path between nodes).

19. As per claim 9, Irwin teaches the system recited in claim 5, wherein the on-chip high-speed interconnect is implemented as a local bus (Col 8, lines 31-35. Bus).

20. As per claim 10, Irwin teaches the system recited in claim 5, wherein the on-chip high-speed interconnect is implemented as a switch (Col 12, lines 20-22. Switch).

21. As per claim 11, Irwin teaches the system recited in claim 5, further comprising an interprocessor high-speed interconnect connecting said plurality of programmable processors and said hardwired logic front end, and an interconnect interface connecting the on-chip high-speed interconnect of each programmable processor to the interprocessor high-speed interconnect (Col 7, lines 44-45; Col 8, lines 28-36; Col 12, lines 30-31. High-speed interconnect connects the plurality of processors and the I/O node. The nodes have a transmission interface connected to the ring.).

22. As per claim 12, Irwin teaches the system recited in claim 11, wherein said hardwired logic front end comprises:

A receiver and a transmitter connect to port logic, said receiver outputting received frame data and said transmitter receiving frame data to be transmitted (Fig, 10, #174. Receive FIFO and Transmits FIFO);

An inbound interface which receives frame data output by said port logic (Fig. 10, #174 "Transmitter"); and

An outbound interface which outputs frame data to be transmitted to said port logic, said inbound interface and said outbound interface being connected to said interprocessor high-speed interconnect (Fig.10, #174. "Receiver" I/O interface receives data and transmits data packets. I/O interface has am inbound interface which receives frame data and a outbound interface which receives packets for output.).

23. As per claim 18, Irwin teaches the system recited in claim 1, wherein said plurality of programmable processors handle network traffic from a first network protocol, performs traffic conversion from the first network protocol to a second network or bus protocol, and handles traffic of the second network or bus protocol (Col 1, lines 13-22. IP router interconnects two different networks.).

24. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin and Adiletta and in view of Hartwell, US Patent #6,629,257.

25. As per claim 13, Irwin does not teach the system recited in claim 12, further comprising a phase locked loop supplying clock signals to said receiver and said transmitter.

26. Hartwell teaches of a phase locked loop supplying clock signals to an input/output (I/O) subsystem (Col 2, lines 29-33).

27. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Irwin and Hartwell because the teachings of Hartwell to use phase locked loop to supply clock signals to the I/O subsystem improves the invention of Irwin by stabilizing communications by keeping it set to a particular frequency.

28. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin and Adiletta and in view of Dwork et al, US Patent #5,513,354 (Dwork hereinafter).

29. As per claim 14, Irwin teaches of monitoring the activity of hardware resources and allocating the work to least loaded processors (Col 6, lines 56-61).

30. Irwin does not teach of re-allocating workload to resources that are not heavily utilized.

31. Dwork teaches an invention for managing tasks in a multiprocessing system, where workload is reallocated to processors, where the workload is balanced among the processors (Col 5, lines 53-56; Col 6, lines 35-38; Col 8, lines 5-9).

32. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Irwin and Dwork because both inventions deal with a multiprocessing system in a ring network. Irwin's invention is to provide high processing utilization, so it would be desirable to reallocate work from a processor that has failed. The teachings of Dwork to reallocate workload to resources that are not heavily utilized improve the efficiency of Irwin's invention by utilizing processing resources.

33. As per claim 15, Irwin, Adiletta, and Dwork taught the system recited in claim 14. Irwin further teaches wherein the built-in monitors examine work queues of said programmable processors (Col 6, line 62-Col 7, line 2. Monitors queues of the processors.).

34. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin, Adiletta, and Dwork and in view of Iwashita et al, US Patent #4,674,034 (Iwashita hereinafter).

35. As per claim 16, Irwin does not specifically teach the system recited in claim 14, wherein the built-in monitors examine memory resources of said programmable processors.

36. Iwashita teaches an invention of a multiprocessor system that provides high-speed processing, where the amount of data stored in the memory is monitored and data input is stopped when the data amount exceeds capacity (Col 16, lines 46-50).

37. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Irwin and Iwashita because both inventions deal with allocating work in a multiprocessing system. Irwin teaches of checking the queue level of the processors to allocate work in order to provide high utilization of the processors. It would be desirable to monitor the memory resources as well. The teaching of Iwashita to monitor the memory resources improves the utilization of the system of Irwin by preventing an overflow in the queue memory.

38. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin, Adiletta, and Dwork and in view of Seaman, US Patent #5,428,766.

39. As per claim 17, Irwin does not teach the system recited in claim 14, wherein the built-in monitors examine interconnection resources of said plurality of programmable processors.

40. Seaman teaches an invention for a multiprocessor system where a monitor examines the bus activity of communications of messages through the buffer memory and the ring memory (Col 9, lines 36-41).

41. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Irwin and Seaman because both inventions deal with a multiprocessor system. The teaching of Seaman to examine the interconnection resources allows the invention of Irwin to regulate the flow of traffic, preventing an inflow of data to a processor.

Conclusion

42. A shortened statutory period for reply to this Office action is set to expire THREE MONTHS from the mailing date of this action.

43. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua Joo whose telephone number is 571 272-3966 and fax number is 571 273-3966. The examiner can normally be reached on Monday to Thursday 8 to 5:30.

44. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on 571 272-3964.

45. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 12, 2005
JJ

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